# Design and tests of the MIDI detector subsystem

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## ABSTRACT

In this paper we present the results of the first tests performed at MPIA on the detector system of MIDI, the Mid-IR interferometric instrument for VLTI. Interferometric observations at 10 $\mu$m, while having advantages with respect to near-IR and optical wavelengths in terms of seeing and coherence time, must face the problem of the strong thermal background coming from the telescope and from the sky. In order to reach background limited performances in the observing conditions foreseen for MIDI at Paranal, the detector and the associated read-out electronics must comply to strict requirements. The different MIDI observing modes are characterized by widely different values of background per pixel; in high background conditions the main problem is to avoid saturation, while in medium-background conditions we are close to read-out noise limited conditions. Therefore, large integration capacity and high speed must be reached with low read-out noise. The read-out electronic chain is described; at maximum speed, one full 16-bit 320×240 pixels$^2$ frame can be read in 3.6 msec. Since only a portion of the detector's field of view will contain useful information, only selected parts of the detector will be read, thus increasing the frame rate. We briefly review the different read-out strategies adopted; the correspondent operations on the detector are described. We also present the results of the first tests performed at MPIA on the whole detector subsystem, using a bare multiplexer of the selected detector (a 320x240 Si:As IBC array from Raytheon Corp.).

**Keywords:** Interferometry, Mid-IR, Electronics, Infrared Detectors

## 1. INTRODUCTION

Ground-based astronomical observations at thermal IR wavelengths are affected by an extremely high background flux compared to the scientific targets. The sources of background radiation are the atmosphere and the telescope optics and infrastructure; all these components are also variable on short timescales (see e.g. Ref 1).

MIDI, the Mid-IR instrument of the Very Large Telescope Interferometer (VLTI),[2] must therefore be able to cope with this high, and time variable background in such a way to minimize the noise on the fringe measurements, which are based on a temporal modulation as well. This implies, in general, the ability to achieve high frame rates, in order to avoid detector saturation and to "freeze" the effects of the atmospheric turbulence.

Moreover, due to the nature of the measurements themselves, a perfect synchronization is needed between the different components of the instrument. In particular, the movement of the MIDI internal delay lines must be exactly synchronized with the acquisition of frames on the detector, in order to relate precisely the data obtained with the value of the Optical Path Delay (OPD) at that moment.

The MIDI Read-Out Electronics (ROE) must therefore be able to:

- read the detector at high speed and with low noise;
- provide a reliable data transfer to the Detector Workstation (DWS), which is designed to perform some real-time preprocessing of the data and give a feedback to the other MIDI subsystems[3]
- synchronize efficiently and reliably with the other components of the instrument, via communication with the DWS and the Delay Line Local Control Unit (DL-LCU).

In the following we will describe the design and the present status of the MIDI detector subsystem; in Sect. 2 we describe the characteristics of the selected detector. We will show then the architecture of the ROE and its realization (Sect. 3), a brief description of the synchronization process (Sect. 4), and finally (Sect. 5) the results of the first tests performed at Max-Planck-Institut für Astronomie (MPIA).

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## 2. THE DETECTOR

The MIDI detector is a Raytheon 320×240 pixel$^2$ Si:As Impurity Band Conduction (IBC) hybrid.[4] It has 50 $\mu$m pixel size with an active area of 98%. The dark current is, for our purposes, negligible (100 $e^-/s$), while the read-out noise (RON) is of about 1000 $e^-$ in high-gain mode (well depth: $1.1 \cdot 10^7 e^-$). This device can be read out both in destructive and non-destructive way, and with two different operational modes: "integrate while read" (IWR) and "integrate then read" (ITR). In both modes, the detector is read-out row by row; in IWR the rows which are not selected for read-out are integrating; the integration time is given therefore by the interval between two reads of the same row. In ITR mode, the integration of the photocurrent into the integration capacitance is controlled by a clock; the integration time is therefore defined by the time in which the photocurrent is actually collected in the integration capacitance. After integration, the detector is read-out. The main differences between the two modes, from the MIDI point of view are:

- IWR allows for the higher frame rates, while ITR can provide the shorter integration times;
- in ITR mode all the pixels integrate during the same time interval, while in IWR, although the integration time is the same, the pixels are not integrating simultaneously.

Windowing is possible by selecting only a part of the rows for read out. This turns out to be particularly useful in the case of MIDI, because in most of the observing modes only a fraction of the detector is actually illuminated. On the other hand, since the number of observing modes (and of illumination patterns) is high, the ROE must be able to load a number of different clock patterns. The spectrum of observing modes is so wide that the detector will work on a range of background fluxes, going from heavily RON-limited to background limited conditions.

Since interferometric observations require a knowledge of the signal modulation (the fringe contrast) and of the source flux (to calibrate the contrast in visibility), a subtraction of the background is necessary. In Ref. 5 are described the different strategies foreseen for the flux calibration. From that discussion it appears clear that another requirement for the detector subsystem is to reach a high stability of the characteristics of the output signal. One of the main goals of the test phase is in fact to investigate the stability of the detector against a number of factors, including temperature variations, flux variations (e.g. due to chopping), frame rate etc.

## 3. THE READ-OUT ELECTRONICS

A scheme of the ROE architecture is shown in Fig. 1.

The ROE is composed of a Front End part (providing biases and clocks, and receiving the output signals), close to the detector, and an Electronics Box containing the Data Acquisition and Control modules. The ROE is then connected to the DWS (a SUN Enterprise 450) which takes over and performs some limited near-real-time preprocessing of the raw data, and stores all the data on disk. The DWS receives from the Observation Software (OS) the parameters needed for the observation, and forwards the settings to the ROE via a serial line.

After readout, the frames are sent by fiber link to a PCD 60 parallel I/O board on the DWS. This kind of link allows the system to manage up to 60 MB/sec, corresponding to a frame time of 2.6 ms for a full, 16-bits, $320 \times 240$ pixels array.

### 3.1. Function of the boards

The different boards shown in Fig 1 are described in the following.

#### 3.1.1. Boards at the dewar

**Clock Driver Board** The clocks and biases signals from the clock-control board are separated and converted to their specific voltage levels in this board. The clock-driver board receives the clock patterns from the Clock Control Board contained in the Read Out Electronics box and switches the appropriate voltage levels which are then sent to the detector. To avoid possible ground loops the incoming clocks are then decoupled by means of optocouplers. The voltages are provided by the bias board and switched to the detector through analog switches; the switch command itself is coming from the optocouplers.

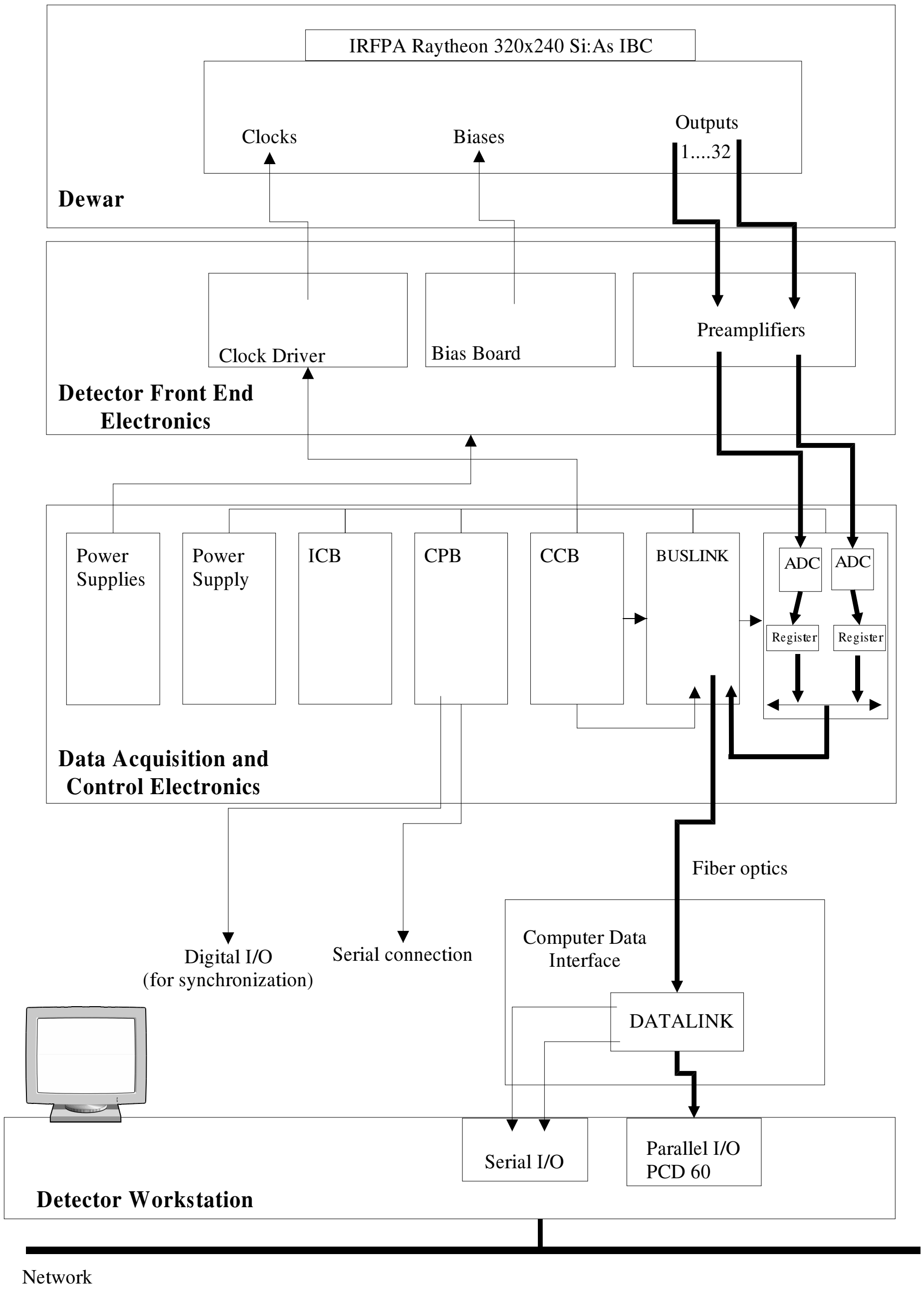


**Figure 1.** Scheme of MIDI Read-Out Electronics

**Preamplifiers** The preamplifiers perform the first amplification of the detector signal, in order to fit the dynamic range of the analog-to-digital converters (ADC). The preamplifier boards (a drawing is shown in Fig. 2) are attached directly to the dewar in order to minimize the length of the wires from the detector outputs to the preamplifiers. The detector can operate both in 16- and 32-outputs mode: in 32 outputs mode, to a given pixel time corresponds a data rate per ADC which is half of that in 16 outputs mode; due to the high rates needed, we use 32 outputs and, therefore, 32 preamplifier stages are needed. Each printed circuit board (PCB) can accommodate 16 stages, so 2

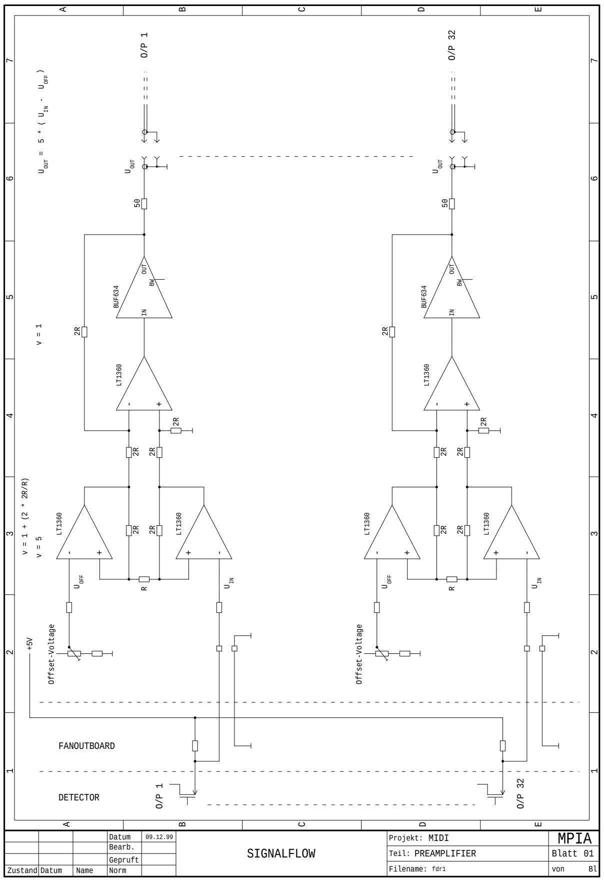


**Figure 2.** Preamplifier circuit

boards are used.

Since the detector signal is superimposed on a common mode voltage, an offset voltage must be provided to compensate it before to go to the ADCs. One offset voltage source can provide variable voltage to 8 amplifier stages; the voltage is in fact distributed to 8 adjustable voltage dividers, so that each output can be compensated individually. In order to distribute the load evenly between both sides of the $\pm 5$ V Power Supply (PS), the offset is trimmed in such a way that for the whole input range the output swing goes from $-2.5$ V to $+2.5$ V.

In the input stage two non-inverting operational amplifiers are used. One is fed with the signal, the other with the offset voltage. The amplified output signals are then fed into a differential stage composed by an operational amplifier and a buffer (the buffer is contained in the feedback loop). The output of the buffer represents the difference between the signal and the offset voltage, which is the detector signal.

After the buffer the signal is fed through the output resistor (50 $\Omega$) to the output coax connector. From here the signal travels down a coaxial cable to the ADC-Board, where the cable is terminated with its characteristic impedance (50 $\Omega$).

**Bias Board** The bias board provides various (negative) voltage levels:

- voltage for the digital clocks;
- power supply for the digital circuitry on chip;

- power supply for the source followers on chip;
- voltages for the remaining biases.

The voltages are generated with 14 adjustable negative voltage regulators (ICL7664). To facilitate a low input-output voltage difference for most of the output voltages, two different input voltages were chosen, providing respectively $-6$ V and $-5$ V. The moderate voltage biases use only the $-6$ V power supply, whereas the most negative biases use the total $-11$ V.

The output voltages are filtered by a special RC-combination which has a low impedance over a wide frequency range. For additional low frequency filtering a 100 $\mu$F Tantalium capacitor is added. To further secure the outputs against static discharges, fast reacting voltage suppressor diodes are provided.

One special circuit had to be added: the clock which controls the DI MOSFET, allowing to switch the detector photocurrent on and off, has to be switched between -4 V and -6 V. The analog switch used has a PS voltage of only -5 V, so it is not possible to provide a -6 V voltage directly with this switch. Two transistors are used to switch the two voltages to the detector; the transistors are operated by the analog switch, which in turn gets its switching signal from the clock board.

#### 3.1.2. Boards at the Electronics box

**Interface Control Board** The Interface Control Board (ICB) contains analog, digital, and RS232 connectors for monitoring, recording and control of system parameters.

**Control Processor Board** The Control Processor Board (CPB) controls the activities of the whole ROE. This is done by means of a Texas Instruments Digital Signal Processor (DSP) TMS 320C30.

The board includes 256K $\times$ 32 bits of programmable memory (EPROM) and 256K $\times$ 32 bits of static RAM. After power-on, the program resident in the EPROM is loaded from there to the RAM and executed there to achieve a faster execution.

The CPB is equipped with to two serial interfaces supporting data rates up to 345600 Baud as well as registers which provide a maximum of 32 bits of parallel I/O. This I/O bits can be used for synchronization purposes. As we will see in Section 4, only three lines are needed to implement the present synchronization concept; the CPB therefore provides an adequate number of digital lines.

**Clock-control board** The selected read-out pattern is loaded by the DSP into the RAM of the Clock Control Board (CCB). It is important to notice that a number of different patterns can be loaded on the DSP and can be used to implement the different read-out modes; in addition, it is possible to load clock patterns via the serial port of the CPB from a remote source, giving to the system a high flexibility.

The read-out is started by a command word written by the CPB into a register of the CCB. The content of the CPB RAM is then shifted to an output register from where the pattern is routed through a buffer to the CCB. The Start Conversion pulse is finally sent to the BUSLINK Board.

**ADC boards** The detector signals coming from the pre-amplifiers are amplified and digitized by 2MHz 16 bit ADCs (Analogic ADC 4322A). Each board has 8 ADCs, so that in total 4 boards are used. A drawing of one ADC board is shown in Fig. 3.

The 2 MHz bandwidth of the ADCs allows in principle a pixel time of up to 250 ns (because in 32 outputs mode the frequency for each output is half the real pixel frequency).

The signal coming from the preamplifier is routed through a coaxial cable with a characteristic impedance of 50 $\Omega$, so the input of the ADC-Board terminates the cable with a 50 $\Omega$ resistor. Following this the signal is fed into a LRC low-pass filter (a $2^{\text{nd}}$ order Butterworth filter).

After the low-pass filter, the signal is amplified by a factor 2 to compensate for the loss due to the voltage divider formed by the two terminating resistors. The output of each amplifier goes to jumpers by means of which the input range of the ADC can be set. Since the signal from the preamplifiers comes with a range of $\pm$2.5 V, the ADC range is

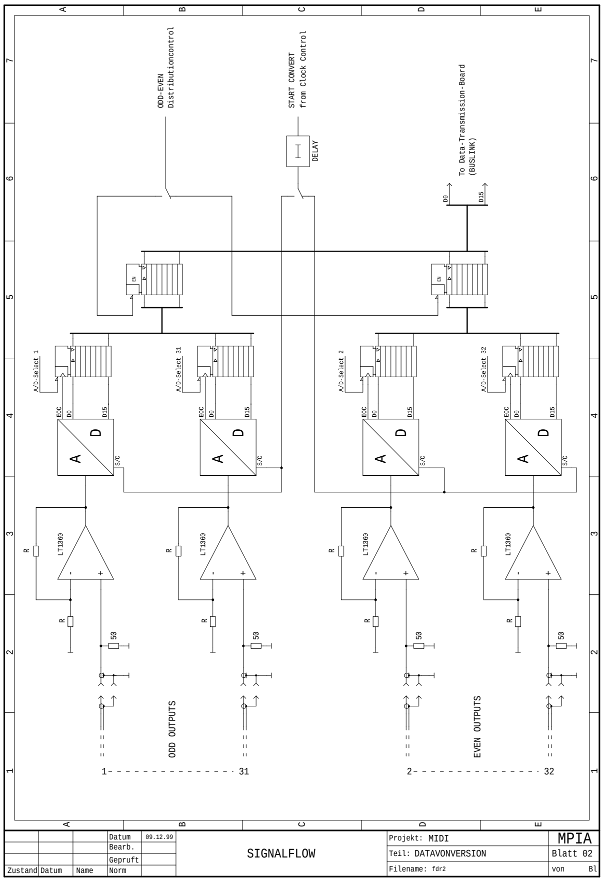


**Figure 3.** ADC board circuit

fixed to this value. The outputs of the ADCs are latched with End of Conversion Pulses into 2x8 D-Type Flip-Flops with 3-State outputs.

The Start Convert Signal is generated on the Clock Control Board together with the other clock pulses. This signal is sent to the BUSLINK board, which creates a Master Start Convert Pulse; the latter pulse is then delayed to take into account the propagation of the clock signals to the detector and of the detector signal through the preamplifiers and the low-pass filters to the ADCs. The Start Convert Signal can be used to control the Analog to Digital conversion and therefore the data output; a possible application of this control would be to avoid data output during idle cycles (see Section 4).

The ADC boards are standard Double Europe boards in width, but are longer; they are composed of an upper and a lower part, each containing 4 ADC4322 and the appropriate circuitry. The two parts are electrically separated to avoid mutual interference.

All ADCs in each part start the conversion simultaneously; the End of Conversion (EOC) signals from all 4 ADCs are combined in a single EOC which is sent to the BUSLINK board through the Backplane Connecting Board. The BUSLINK board then will start to read the data and to sent them to the DWS.

**BUSLINK board and Backplane Connecting Board** The BUSLINK board controls the read-out of the ADC boards and the data transfer via fiber optics (DATALINK) to the data-interface on the DWS. The BUSLINK receives the Start Conversion Pulse and generates a Master Start Convert Pulse which is sent to the Backplane Connecting Board (see below).

Due to the detector's architecture, only 16 outputs are read simultaneously: the 32 outputs are accommodate in such a way that all 4 boards are converting at the same time, alternatively with their upper and the lower part. The switch between the upper parts (odd columns) and the lower parts (even columns) is performed by a flip-flop. The flip-flop is reset to the "odd" state by the "row start" pulse of the read-out pattern.

The Backplane Connecting Board links the clocks with the ADC Boards; it receives the Master Start Convert pulse and transfers it to the ADCs, with a delay set by a delay line. This solution was preferred to using a clock pulse, because the delay line solution gives a better time resolution, and therefore allows one to better match the delay needed.

### 3.1.3. Boards at workstation

**Data Interface** The Data Interface reconverts the optical signal from the fiber-pair again into 3 serial channels and the 16 bit parallel data and transmits them to the I/O connections of the workstation.

## 4. SYNCHRONIZATION

A critical issue in operating MIDI is to synchronize the detector read-out, the start and end of each elementary integration, with the rest of the MIDI instrument, in particular with the Delay lines which are used to scan the fringe pattern.

Three synchronization lines are implemented:

- READY/NOT-READY state line from ROE to the Delay Lines Local Control Unit (DL-LCU);
- START/PAUSE state line from DL-LCU to ROE;
- FRAME start/FRAME end state line from ROE to DL-LCU (in case of ITR it could also be needed a Global RESET / end integration state line).

The READY state is needed to tell the DL-LCU that the ROE is ready to take data, so that the DL-LCU can send the START state to enable the start of the data taking, when it receives the OK status from the other subsystems (Delay lines settling, chopping settling, or other synchronizations).

The NOT-READY state is needed to inform the LCU when for any reason the ROE has paused or stopped the data taking, so that further processing with delay lines and chopping can paused. The 2 GB data-stream limit, imposed by the present architecture, could also need short pausing between full ramp-cycles.

The START state from the ROE will give a confirmation of the start of an observing sequence, or it could be used to give the DL-LCU a timing to start acquisition synchronized with the ROE. Here it depends from the RO-mode, whether the DL-LCU has to synchronize each single frame, or after some frames, or only after the end of a ramp/step cycle. So the PAUSE state enables the DL-LCU to trigger exactly the timing. If the DL-LCU wants to break the acquisition, it goes to PAUSE state and sends a break signal. The START/PAUSE line is needed in any case, independently of the strategy actually used in the final concept.

The near-realtime readjustment of the Delay Lines, as well as the state of chopping, nodding, tip-tilt and (in a later phase) of the fringe tracker, must be synchronized.

The START FRAME and END FRAME signals from the ROE are needed in order to allow the LCU to:

- receive an acknowledgement, when the frames are really completed
- build a time-table for all frames start/end during test phases (SPARC timing is in the order of 10 ms exact for small times or less depending from load)
- have a fast response at cycle-ends for moving delay lines, etc.

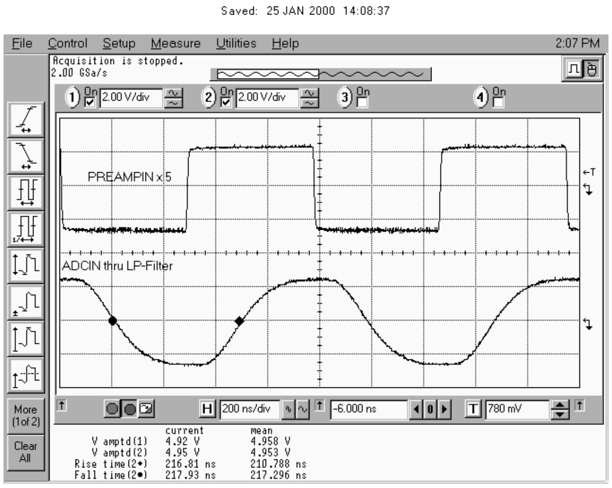


**Figure 4.** Response of the low-pass filters before the ADCs

Because of possible synchronization at start time with the idle modes of the detector, this might be very important.

For example: for a new setup of the detector read-out there might be a need to wait for some idles cycles of the detector, to come into stable conditions. So the idle mode might be similar to the read-mode, but without reading data or reading data frames without processing them. The following read sequence would probably be best started in synchronization of the timing of the current idle mode, to keep the detector thermally stable.

In the ITR mode the Global Reset signal or the integration start signal should be given to the DL-LCU, and the end of the integration time signal will inform the DL-LCU that movement of delay-lines or other actions can already be started during the read-out of the data frame. In this way, the knowledge of the frame activity will help to design the concept in an optimized way and to be ready for possible fast reactions on the sure path.

### 4.1. Idle modes

Idle modes (in which the detector is read out without actually acquiring data) are required to keep the detector thermally stable during short pauses between different observing blocks. In our concept, idle modes are normally started automatically after the end of the cycle-repeats and normally adapted to the same or similar read-out scheme like the current read-out setup, but without delivering data. To perform this task, the fastest possibility is to use the switches which enable the ADC converters. This option has also the smallest impact on the stability of the detector.

In some observing modes, idle modes could be required also within an observing cycle. the single cycle ( 1 complete step/ramp cycle), for example moving the chop-mirror in 250ms, the detector should also run in idle mode. At other cycle ends (for ex. real time self fringe tracking) the pause should not be filled with idle modes, because after a few ms the next read-out would be started again,

## 5. PERFORMANCES AND TESTS

The first tests which had been performed were the check of the clock board operation, and the verification of the frequency response of the low-pass filters in front of the ADCs.

After realization of the clock boards, the first version of the clock patterns was loaded and run. The corresponding output has been checked to verify the correct response of the boards. This tests have been made at different pixel speeds to prove the ability to provide clean signals at the pixel speeds foreseen for operation. The maximum speed for each memory cell is currently 66 ns, which allows to reach a pixel time of 330 ns. The low-pass filters currently used before the ADCs limits the pixel time to 670 ns. Figure 4 shows the effects of the low-pass filter on an input signal at 1 MHz coming from a pulse generator. It can be seen that the response of the present filter is not satisfactory at this speed. The low-pass filters are being modified to allow at least a pixel time of 500 ns, which is necessary to

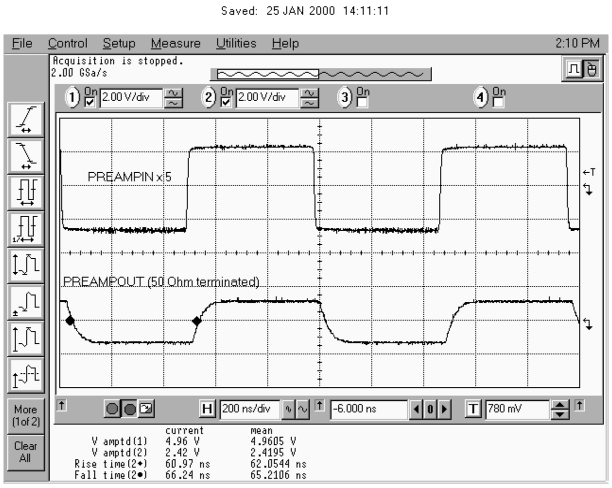


**Figure 5.** Response of the preamplifiers

meet the speed requirements for all the foreseen observing modes. The minimum integration time achievable by the ROE, in fact, is determined basically by the speed of the fast clocks (which control the scanning of the columns in a row) and by the duration of the settling time in the Sample and Hold circuit on the chip. With the values presently adopted (pixel time of 500 ns, and 5 $\mu$s settling time per row) the minimum integration time per a full frame is 3.6 ms. Since all the scientific modes require only to read out a portion of the array, the actual minimum integration time will be smaller than this number.

The preamplifiers have also been tested at the frequencies of operation, to verify the frequency response. In Fig. 5 it is shown the response of the preamplifiers to a given input signal at 1 MHz. In this case, the frequency response appears satisfactory.

An important verification consists in measurements of the noise produced by the ROE. Since we want our RON performance to be determined by the intrinsic characteristics of the array, we must not be limited by the noise associated to the ROE. Our goal is to get at most 1000 $e^-$ RON, which means to have a noise from the ROE smaller than 200 $\mu$V. These tests are now starting.

The first phase of our experiments involves the first operations on the bare multiplexer; this can be done at room temperature. This phase started in February, 2000. We used a test fanout board from J. K. Henricksen and associates; this board was not populated, so we added the passive components needed; the detector is clamped to the socket by a mechanical mount which was produced at MPIA, and that can be used at cryogenic temperature. The first tests (at room temperature) can be used only to verify the correctness of the clocking patterns and of the readout chain. The first light image is shown in Fig. 6. The main activities in this phase can be summarized as follows:

- tests of the read out electronics. By using a mask with a recognizable pattern, and exploiting the sensitivity of the multiplexer to visible light, we can verify that the clock patterns and the whole read out electronics chain produce a correct image, and that the multiplexer itself is working correctly; in addition to these tests, we will be able to verify the ability of the whole ROE chain to manage the data flow generated at maximum speed
- implement and test the different read-out strategies envisaged for operations; snapshot, integrate while read, non-destructive read-out, and the windowing capabilities. Once the general schemes will be realized, all the subsequent fine tuning modifications will require minor changes in a few timings.
- In tests made at cryogenic temperatures, we will start verifying the RON performances, and the linearity of the on-chip signal chain. This will be done, for instance, by feeding a clocked signal into the reset bias; this will simulate a signal and, by measuring the output corresponding to different signal levels, we could measure

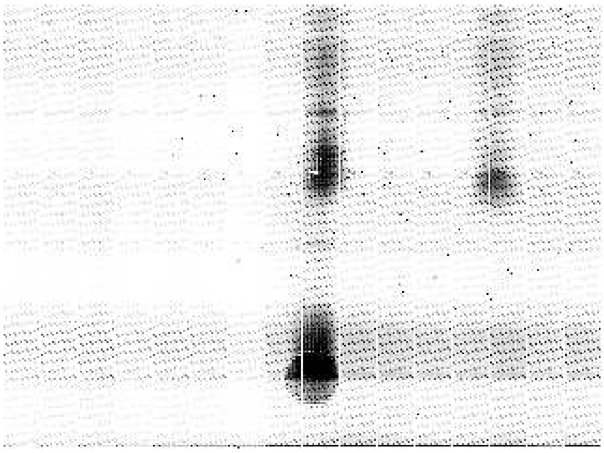

**Figure 6.** The first light image obtained with the multiplexer

the linearity. The same measurements will be done at different speeds, in order to verify, for instance, the sensitivity to a short settling time in the detector's Sample and Hold circuits; on one hand, in fact, it is necessary to minimize the duration of the SH pulse in order to be able to reach high frame rates, while on the other we don't want to lose in linearity and dynamical range

The following test phase, scheduled to start in March, 2000, will involve the operation of an engineering grade device, which has been already delivered to MPIA by Raytheon Corp.

## 6. CONCLUSIONS

We conclude by comparing the main requirements set for the MIDI Detector Subsystem with the performances achieved (or foreseen) by the detector's characteristics and by the ROE.

- Read-Out Noise: the goal is to reach at least the performances assumed in computing the instrument sensitivity: 1000 electrons in high gain mode, with a full well depth of $1.1 \cdot 10^7 e^-$, which are also the design performances provided by Raytheon. By using a quieter ROE and, whenever possible, non-destructive readout, we could reach even better performances;
- Read speed: our hardware has the ability to reach a minimum integration time (in IWR mode) of about 3.6ms, which is within the requirements (4ms in Fourier mode, see Ref. 5);
- Flexibility: we can define and download a virtually unlimited number of clocking patterns, which allow us to accommodate the relatively large number of different observing modes and subframes foreseen for operation;
- Synchronization: the DSP digital I/O lines provide a large number of status line, more than enough for the needed synchronisation.

## ACKNOWLEDGMENTS

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